

1/5’’ UXGA CMOS Image Sensor

GC2145 CSP

DataSheet
V1.1

2014-12-15

GalaxyCore Inc.

Revision History

Version 1.0 2013.12.01

- Document Release

Version 1.1 2014.04.29

- Add D-PHY LP Transmitter DC specifications
- Add DC Parameters

Version 1.1 2014.05.21

- Update CRA

Version 1.1 2014.07.21

- Update power off sequence

Version 1.1 2014.09.18

- Update Serial Bus Timing

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- Update DC Parameters

Version 1.1 2014.12.15

- Update DC Parameters

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1. Sensor Overview

1.1. General Description

GC2145 is a high quality 2Mega CMOS image sensor, for mobile phone camera applications and digital camera products. GC2145 incorporates a 1616V x 1232H active pixel array, on-chip 10-bit ADC, and image signal processor.

According to different light conditions , The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control .Besides , interpolation, de-noise, and color correction, gamma correction are supported, which can revert the real scene better. The sensor also provides various data formats, such as Bayer RGB, RGB565, YCbCr 4:2:2. Internal master clock can be generated by on-chip Phase Lock Loop(PLL) oscillator.

1.2. Features

- Standard optical format of 1/5 inch
- Various output formats: YCbCr4:2:2, RGB565, Raw Bayer
- Power supply requirement : AVDD: 2.7~3.0V
  DVDD: 1.7~1.9V
  IOVDD: 1.7~3.0V
- PLL support
- Windowing support
- MIPI interface support: Single lane/Double lane(CSI-2 V1.0/PHY-1.0)
- Horizontal /Vertical mirror
- Image processing module
- Package: CSP/COB/wafer

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1.3. Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment
- Security systems
- Industrial and environmental systems

1.4. Main Characteristics

Parameter	Typical value
Optical Format	1/5 inch
Pixel Size	1.75μm x 1.75μm
Active pixel array	1616 x 1232
Shutter type	Electronic rolling shutter
Max Frame rate	UXGA : 30fps@168MHz, DCLK 720P : 30fps@96MHz , DCLK SVGA : 30fps@120MHz, DCLK
Power Supply	AVDD: 2.7~3.0V DVDD: 1.7~1.9V IOVDD: 1.7~3.0V
Power Consumption	180mW(Active) <200uA(Standby)
SNR10	< 70Lux
Dark Current	4.2 mv/s
Sensitivity	1200mV/Lux.sec
Operating temperature	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	25º(non-linear)
Package type	CSP/wafer/ COB
Input reference clock	6~27MHz

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2. DC Parameters

2.1. Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	1	40	uA
Digital	I_{DVDD}	—	6	100	uA
I/O	I_{IOVDD}(1.8V)	—	25	40	uA
	I_{IOVDD}(2.8V)	—	35	60	uA

INCK: 24MHz, RST: H, PWND: H
Typ. Analog: 2.8V, Digital:1.8V, Tj=25℃

2.2. Operation current

2.2.1 Parallel mode

Full size Operation Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	25	50	mA
Digital	I_{DVDD}	—	40	70	mA
I/O	I_{IOVDD}(1.8V)	—	20	40	mA
	I_{IOVDD}(2.8V)	—	25	50	mA

Full Pixel 20 frame/s YCbCr output
DCLK: 120M
Typ. Analog:2.8V, Digital:1.8V, Tj=25℃

720P Operation Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	25	50	mA
Digital	I_{DVDD}	—	28	55	mA
I/O	I_{IOVDD}(1.8V)	—	20	40	mA
	I_{IOVDD}(2.8V)	—	25	50	mA

720P 30 frame/s YCbCr output
DCLK: 96M
Typ. Analog: 2.8V, Digital: 1.8V, Tj=25℃

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2.2.2MIPI mode

Full size Operation Current (MIPI mode)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	25	50	mA
Digital	I_{DVDD}	—	65	80	mA
I/O	I_{IOVDD}(1.8V)	—	1	3	mA
	I_{IOVDD}(2.8V)	—	1.5	4	mA

Full Pixel 30 frame/s YCbCr output 672Mbps
DCLK: 168M
Typ. Analog:2.8V, Digital:1.8V, Tj=25℃

720P Operation Current(MIPI mode)

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	25	50	mA
Digital	I_{DVDD}	—	40	70	mA
I/O	I_{IOVDD}(1.8V)	—	1	3	mA
	I_{IOVDD}(2.8V)	—	1.5	4	mA

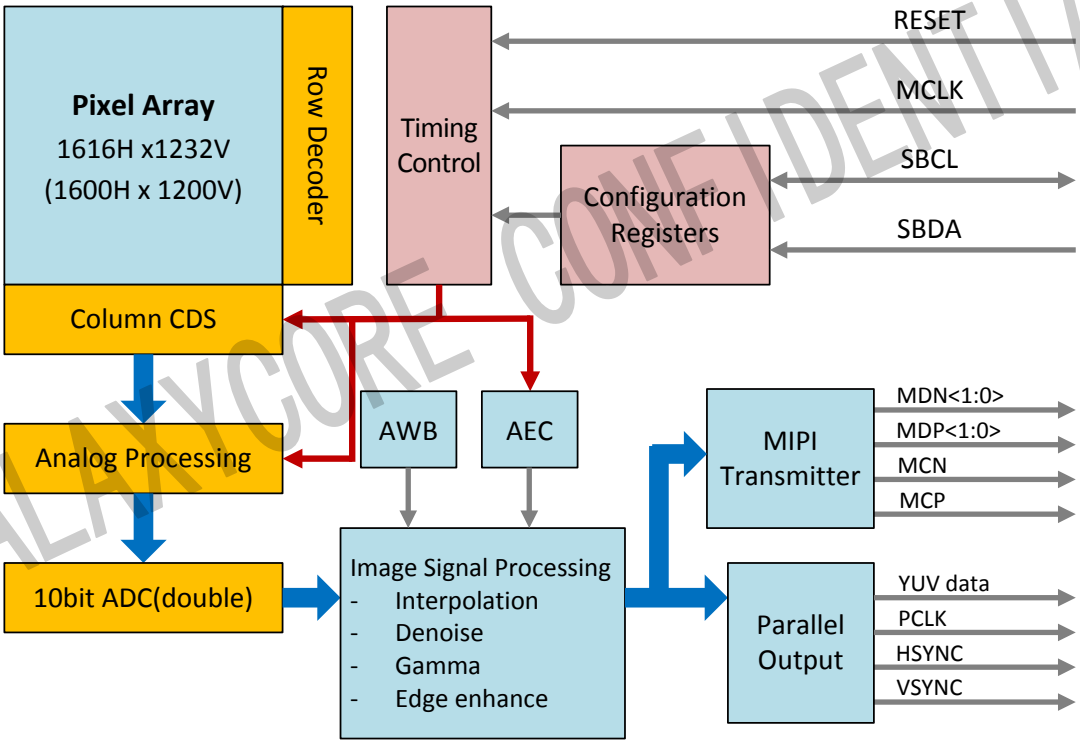
720P 30 frame/s YCbCr output 384Mbps
DCLK: 96M
Typ. Analog:2.8V, Digital:1.8V, Tj=25℃

2.3. DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	**V_{AVDD}**	2.7	2.8	3.0	V
	V_{DVDD}	1.7	1.8	1.9	V
	V_{IOVDD}	1.7	1.8	3.0	V
Digital Input(Conditions: AVDD = 2.8V, DVDD = 1.8V, IOVDD = 1.8V)					
Input voltage HIGH	**V_{IH}**	1.4			V
Input voltage LOW	**V_{IL}**			0.6	V
Digital Output(Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	**V_{OH}**	1.6			V
Output voltage LOW	**V_{OL}**			0.2	V
D-PHY LP Transmitter DC specifications					
Thevenin output high level	**V_{OH-LP}**	1.1	1.2	1.3	V
Thevenin output low level	**V_{OL-LP}**	-0.5		0.5	V

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3. Block Diagram

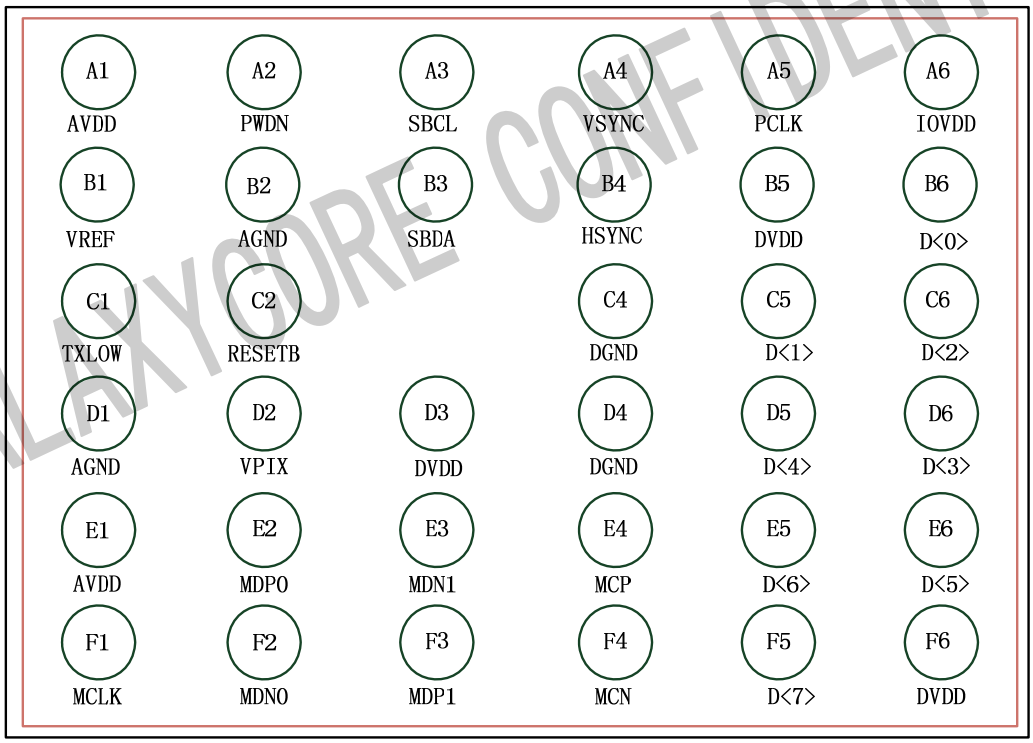


GC2145 has an active image array of 1616 x 1232 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, de-noise, and color correction, gamma correction, and data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

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4. CSP Package

4.1. Pin Diagram



Top view

4.2. Signal Descriptions

	Name	Pin type	Description
A1	**AVDD**	Power	Power for analog circuit/sensor array
A2	**PWDN**	Input	power down (active high)
A3	**SBCL**	Input	SCCB input clock
A4	**VSYNC**	Output	Vertical reference output
A5	**PCLK**	Output	Pixel clock output
A6	**IOVDD**	Power	Power Supply for I/O circuits
B1	**VREF**	Power	Internal power
B2	**AGND**	Ground	Ground for analog circuit

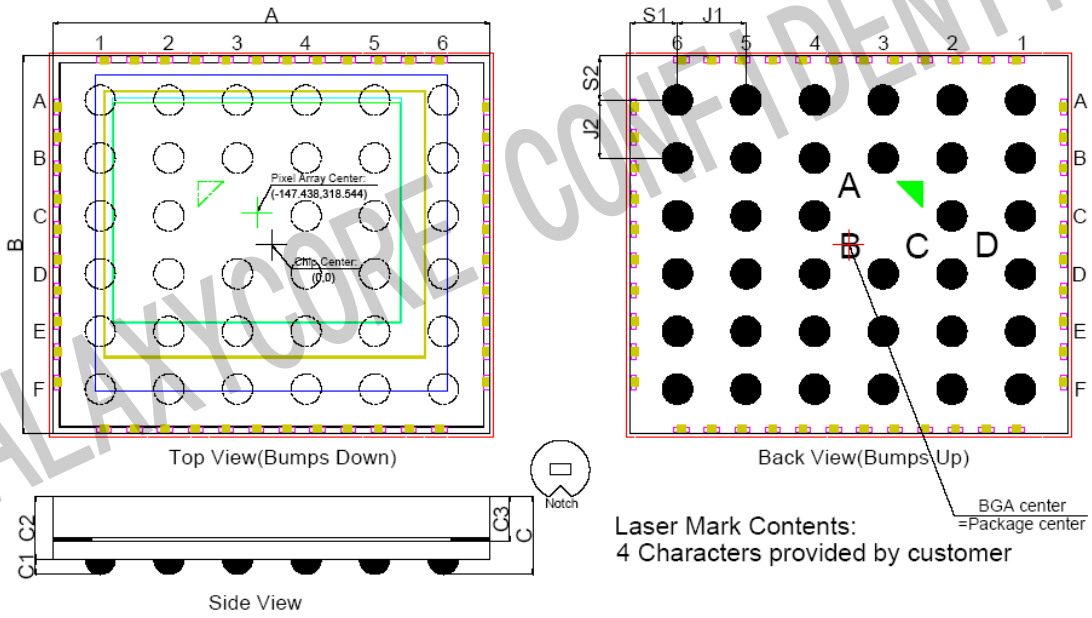
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B3	**SBDA**	I/O	SCCB data
B4	**HSYNC**	Output	Horizontal sync output
B5	**DVDD**	Power	Power for digital core
B6	**D<0>**	Output	YUV/RGB video port bit [0]
C1	**TXLOW**	Power	Internal power
C2	**RESETB**	Input	reset (active Low)
C3	**NC**		
C4	**DGND**	Ground	Ground for digital circuit
C5	**D<1>**	Output	YUV/RGB video port bit [1]
C6	**D<2>**	Output	YUV/RGB video port bit [2]
D1	**AGND**	Ground	Ground for analog circuit
D2	**VPIX**	Power	Internal power
D3	**DVDD**	Power	Power for digital core
D4	**DGND**	Ground	Ground for digital circuit
D5	**D<4>**	Output	YUV/RGB video port bit [4]
D6	**D<3>**	Output	YUV/RGB video port bit [3]
E1	**AVDD**	Power	Power for analog circuit/sensor array
E2	**MDP0**	Output	MIPI Data<0> (+)
E3	**MDN1**	Output	MIPI Data<1> (-)
E4	**MCP**	Output	MIPI clock (+)
E5	**D<6>**	Output	YUV/RGB video port bit [6]
E6	**D<5>**	Output	YUV/RGB video port bit [5]
F1	**MCLK**	Input	Sensor master input clock
F2	**MDN0**	Output	MIPI Data<0> (-)
F3	**MDP1**	Output	MIPI Data<1> (+)
F4	**MCN**	Output	MIPI clock (-)
F5	**D<7>**	Output	YUV/RGB video port bit [7]

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F6	**DVDD**	Power	Power for digital core

5. Package Specifications

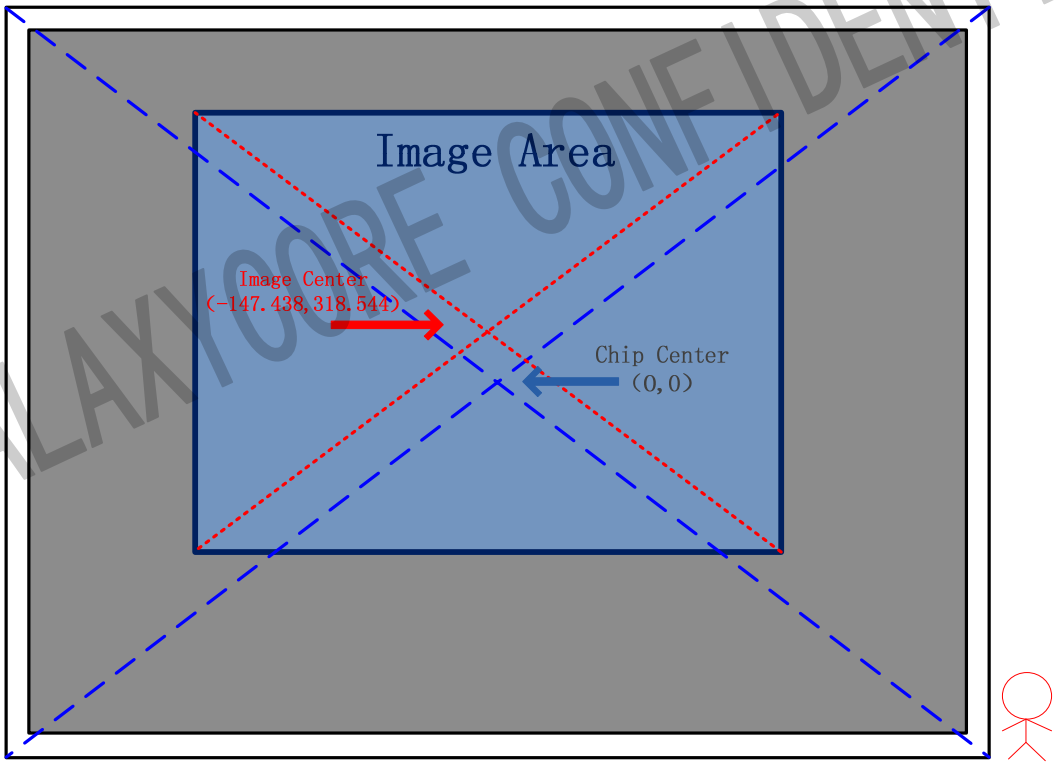


Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	4.330	4.305	4.355
Package Body Dimension Y	B	3.720	3.695	3.745
Package Height	C	0.750	0.690	0.810
Ball Height	C1	0.160	0.130	0.190
Package Body Thickness	C2	0.590	0.555	0.625
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465
Ball Diameter	D	0.300	0.270	0.330
Total Ball Count	N	35		
Pins Pitch X axis	J1	0.680		
Pins Pitch Y axis	J2	0.570		
Edge to Pin Center Distance along X	S1	0.4650	0.435	0.495
Edge to Pin Center Distance along Y	S2	0.4350	0.405	0.465

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6. Optical Specifications

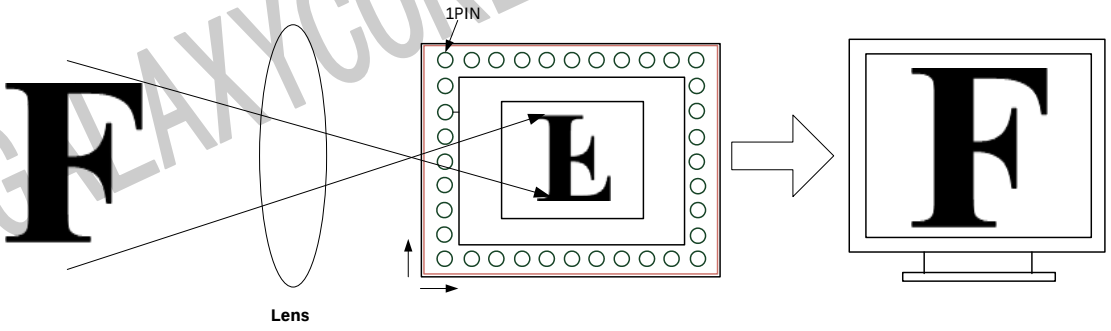
6.1. Sensor Array Center



Top View

6.2. Readout Position

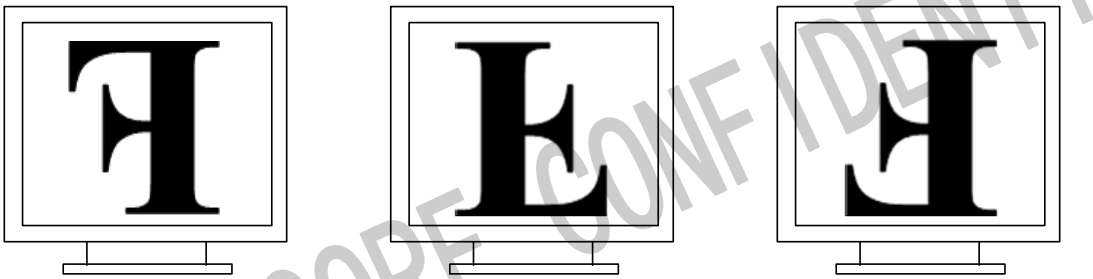
The 2355 default status is readout from the lower left corner with pin 1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so proper image output results when Pin 1 is located in the upper left corner.



In addition, this system supports up/down and/or right/left inversion, and is capable of following outputs. When using the inversion function, the pixel array read from the

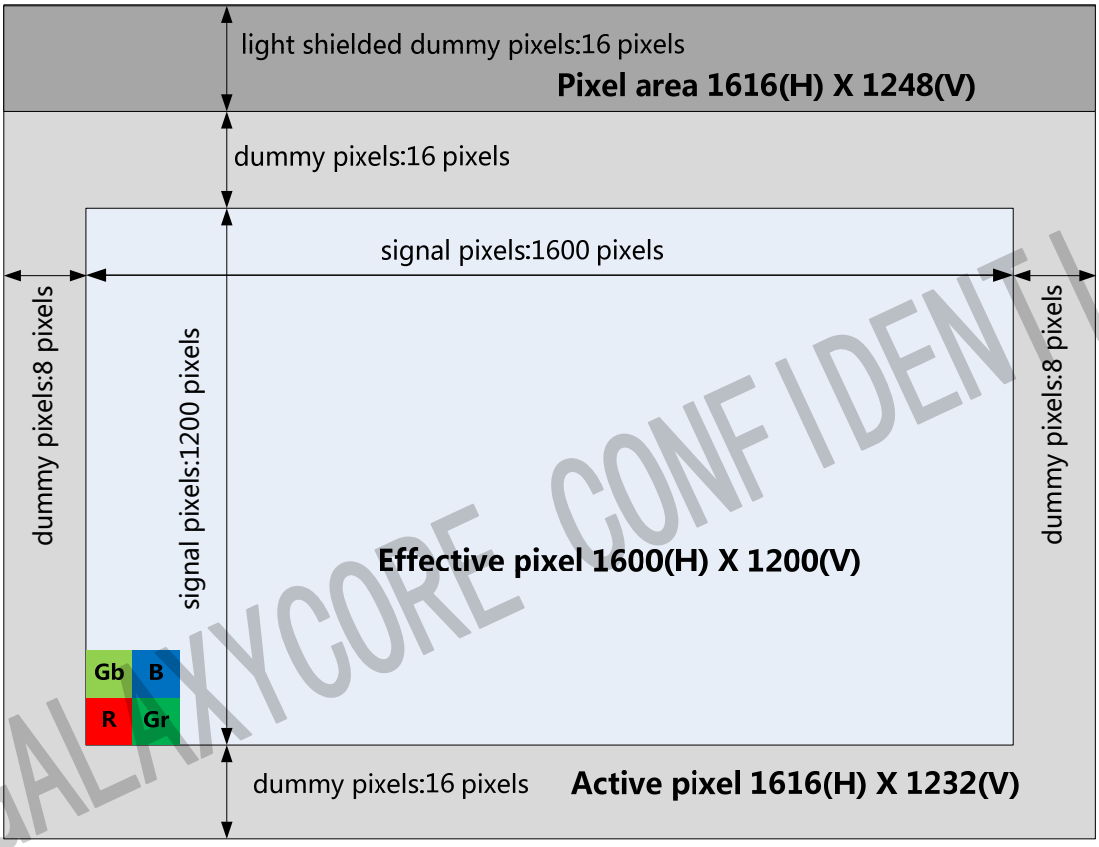
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sensor changes, but this is processed adaptively within the ISP, so there is no need for users to be aware of it. However, care must be taken in RAW output mode, as the sensor data is output as is.



Horizontal Mirror　　Vertical Flip　　Horizontal Mirror and Vertical Flip

6.3. Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 1615. If flip in column, column

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is read out from 1615 to 0.

6.4. Lens Chief Ray Angle (CRA)

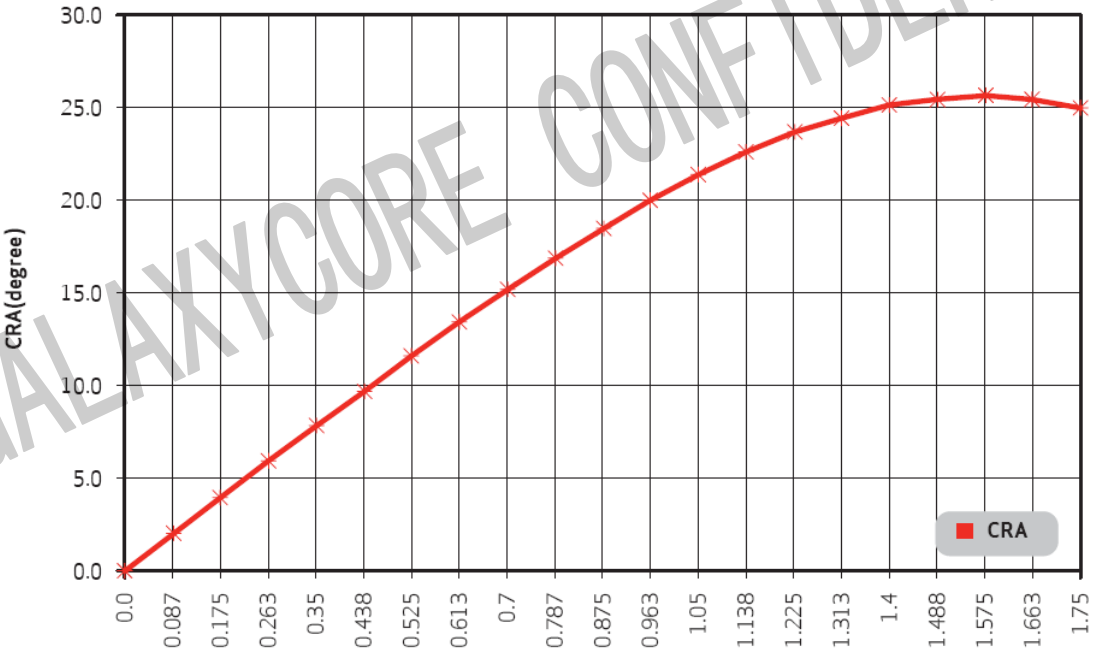


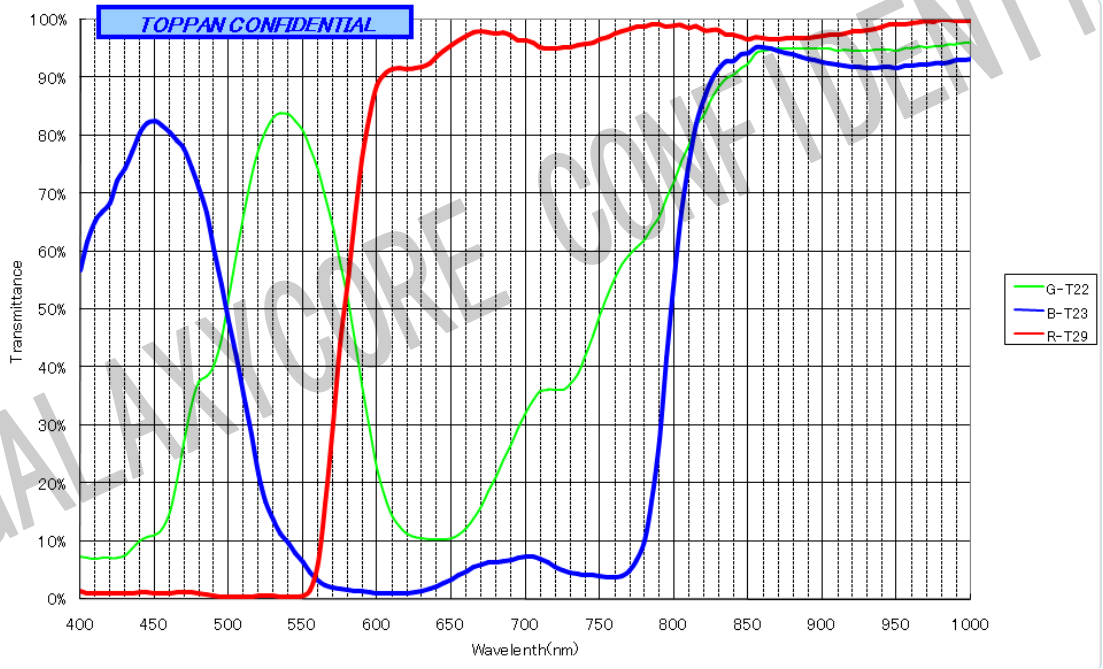
Image Height (mm)

Field (%)	Image height(mm)	CRA(degrees)
0	0	0
10	0.175	3.9
20	0.350	7.8
30	0.525	11.6
40	0.700	15.2
50	0.875	18.5
60	1.050	21.4
70	1.225	23.7
80	1.400	25.2
90	1.575	25.7
100	1.75	25.0

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6.5. Color Filter Spectral Characteristics

The optical spectrum of color filters is shown as follows:



7. Two-wire Serial Bus Communication

GC2145 Device Address:

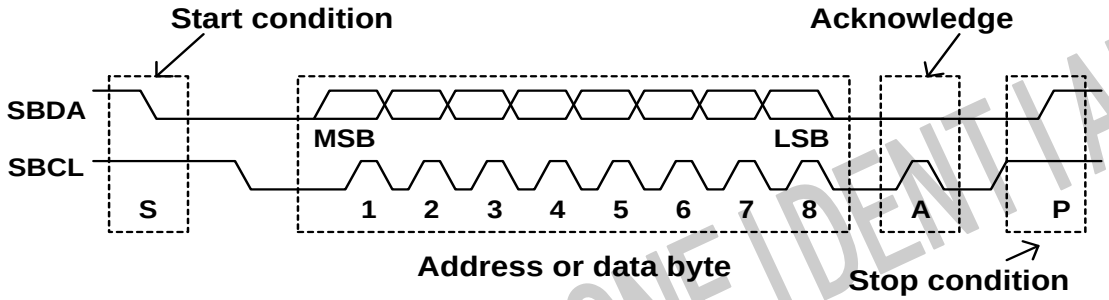
serial bus write address = 0x78, serial bus read address = 0x79

7.1. Protocol

The host must perform the role of a communications master and GC2145 acts as either a slave receiver or transmitter. The master must do:

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**

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Single Register Writing:

S	78H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	78H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	78H	A	Register Address	A	S	79H	A	Data	NA	P

Notes:

From master to slave

From slave to master

S: Start condition

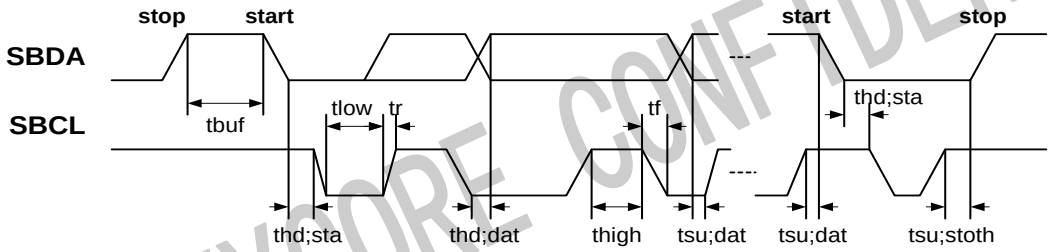
P: Stop condition

A: Acknowledge bit

NA: No acknowledge

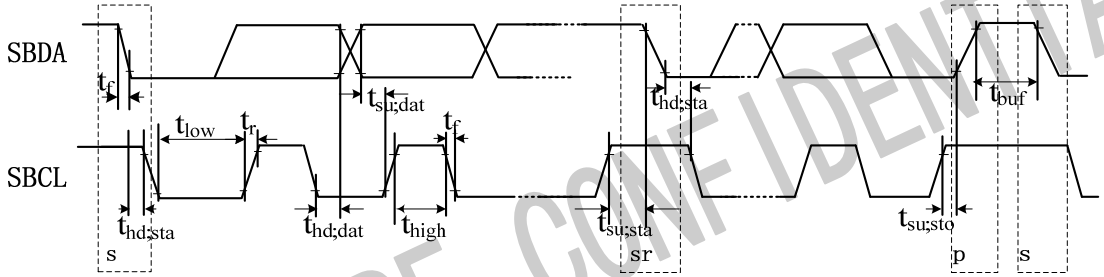
Register Address: Sensor register address

Data: Sensor register value



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7.2. Serial Bus Timing



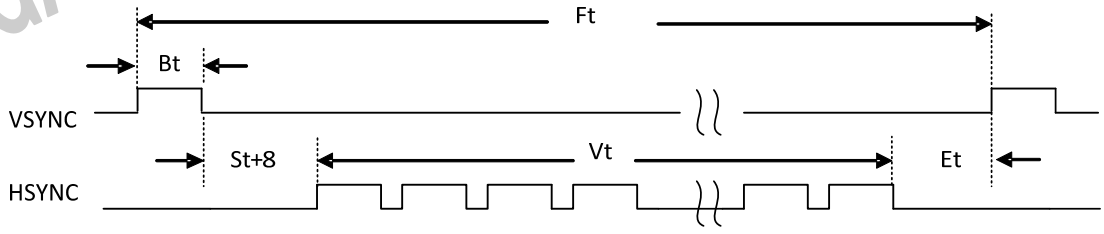
Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

8. Applications

8.1. Timing

7.1.1 Parallel

Supposed VSYNC is LOW active and HSYNC is HIGH active, and output format is YCbCr/RGB565, then the timing of VSYNC and HSYNC is following:



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Ft =VB+ Vt +8 (unit is row_time)

VB = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

- Ft -> Frame time, one frame time.
- Bt -> Blank time, VSYNC no active time.
- St -> Start time, setting by register P0:0x13
- Et -> End time, setting by register P0:0x14
- Vt -> valid line time. UXGA is 1200, Vt=win_height-8, win_height is setting by register P0:0x0d and P0:0x0e(1232).

When exp_time <= win_height+VB, Bt=VB-St-Et. Frame rate is controlled by window_height+VB.

When exp_time > win_height+VB, Bt=exp_time-win_height-St-Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = Hb + Sh_delay + win_width/2 + 4.

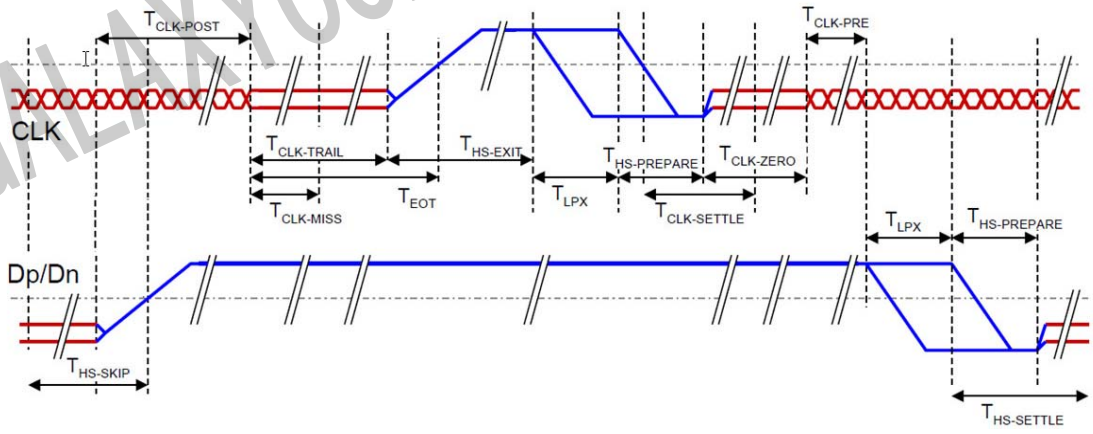
Hb –> HBlank or dummy pixel, Setting by register P0:0x05 and P0:0x06.

Sh_delay -> Setting by register P0:0x11[9:8], P0:0x12[7:0].

win_width -> Setting by register 0x0f and P0:0x10, win_width = 1600, final_output_width + 8. So for UXGA, we should set win_width as 1616.

7.1.2 MIPI

Clock lane low-power



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Notice:

- Clock must be reliable during high speed transmission and mode-switching
- Clock can go to LP only if data lanes are in LP(and nothing relies on it),
- In Low –Power data lanes are conceptually asynchronous(independent of the high speed clock)

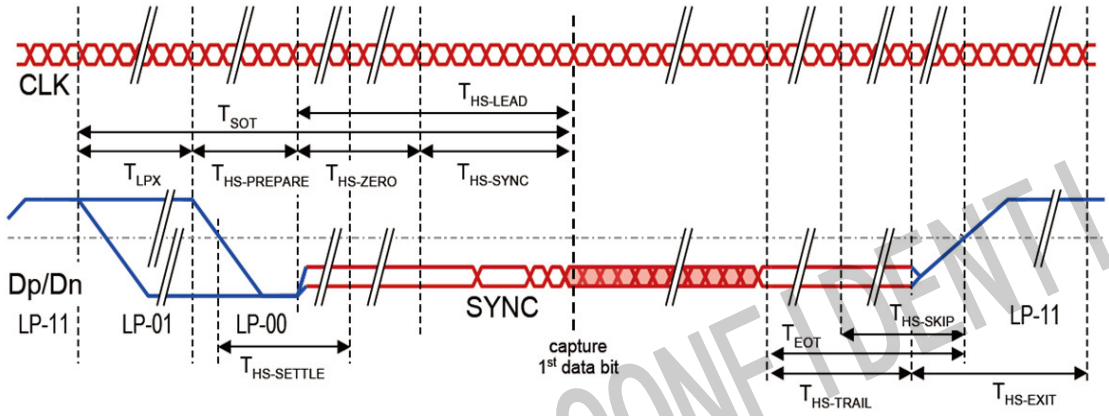
  T_{CLK_PRE}: setting by Register P3: 0x24

  T_{CLK_POST} : setting by Register P3: 0x25

  $T_{CLK\text{-}ZERO}$: setting by Register P3: 0x23

  T_{CLK_TRAIL}: setting by Register P3: 0x26

Data Burst



Notice:

- Clock Keeps running and samples data lanes(except for lanes in LPS)
- Unambiguous leader and trailer sequences required to distill real ditz,
- trailer is removed inside PHY(a few bytes)
- Time-out to ignore line values during line state transition

  T_{LPX} : setting by Register P3:0x21

  $T_{HS\text{-}PREPARE}$: setting by Register P3: 0x29

  $T_{HS\text{-}ZERO}$: setting by Register P3:0x2a

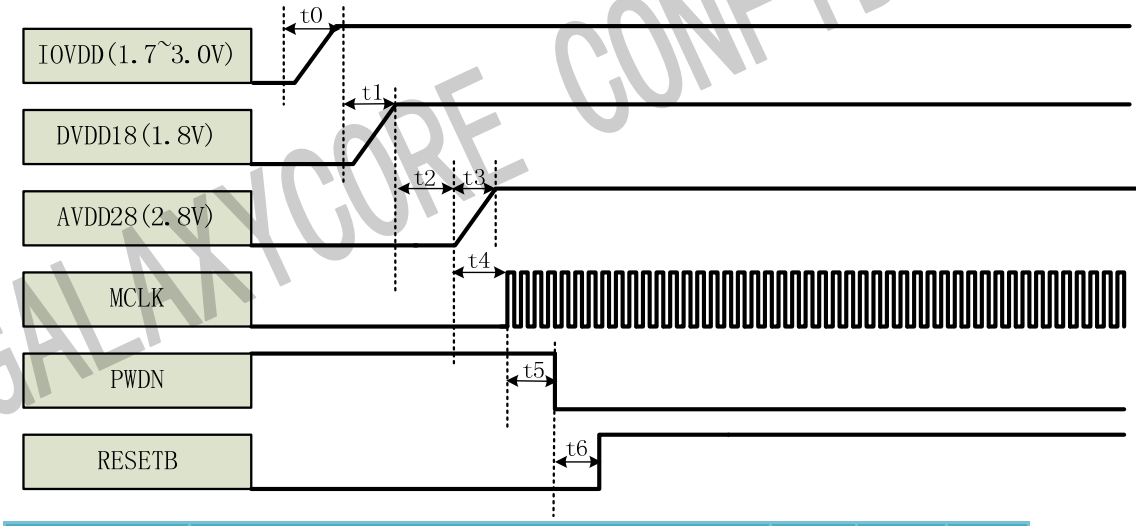
  $T_{HS\text{-}TRAIL}$: setting by Register P3:0x2b

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$T_{HS-EXIT}$: setting by Register P3: 0x27

8.2. Power On/Off Sequence

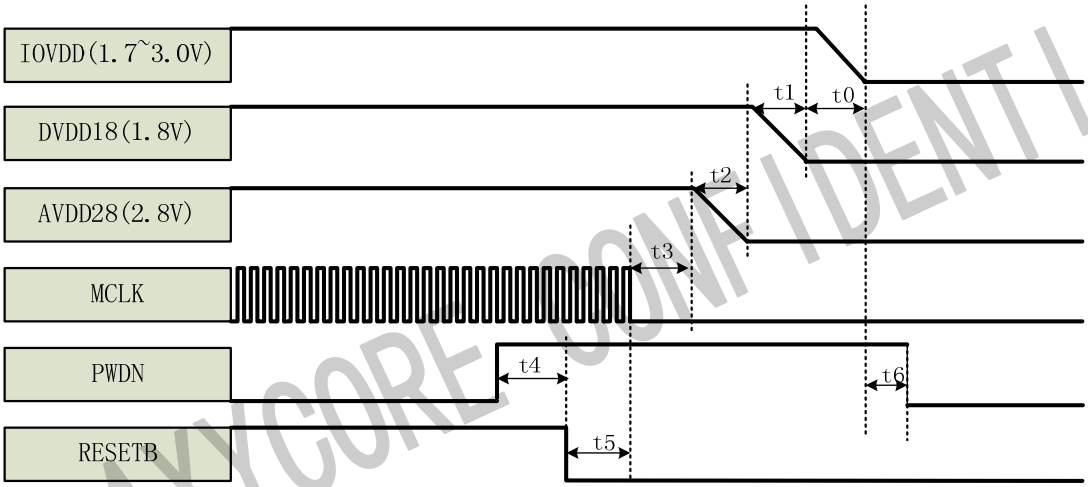
7.2.1 Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	50		us
t1	From IOVDD to DVDD	0		us
t2	From DVDD to AVDD	50		us
t3	AVDD rising time	50		
t4	From AVDD to MCLK applied	0		us
t5	From MCLK applied to Sensor enable	0		us
t6	From PWDN pull low to RESET pull high	0		us

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7.2.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD to IOVDD falling time	0		us
t1	From AVDD to DVDD falling time	0		us
t2	AVDD falling time	0		us
t3	From MCLK disable to sensor AVDD power down	0		us
t4	From sensor disable to RESET pull low	0		us
t5	From sensor RESET pull low to MCLK disable	0		us
t6	From power Off to PWDN pull low	0		us

✧ **Recommended power on/off sequence is above.**

9. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	chip_ID[15:8]	8	0x21	RO	chip_ID[15:8]
0xf1	chip_ID[7:0]	8	0x45	RO	chip_ID[7:0]
0xf2	pad_vb_hiz_mode data_pad_io sync_pad_io	8	0x0f	RW	[4] auto vb pad hiz [3] data_pad_io [2:0] sync_pad_io 0:input 1:output
0xf3	I2C_open_en	1	0x01	RW	[0] I2C_open_en
0xf6	Up_dn Pwd_dn	3	0x00	RW	[5:4] up_dn 00: not pull 01: pull down

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					10: pull up 11: illegal [0] PWD dn 0: pull down 1: not pull
0xf7	PLL_mode1	8	0x05	RW	[7] dvp mode [6:4] serial_clk_double [3] clk_double [2] NA [1] div2en [0] pll_en
0xf8	PLL_mode2	8	0x81	RW	[7] pll_dgdiv_en [6] NA [5:0] divx4
0xf9	cm_mode	8	0xfe	RW	[7] regf clk enable [6] 2pclk enable [5] pclk enable [4] hpclk enable [3] isp all clock enable [2] serail_clk enable [1] re_lock_pll [0] not_use_pll
0xfa	clk_div_mode	8	0x11	RW	[7:4] divide_by [3:0] clock duty eg:pllclk=192
0xfb	I2C_device_ID	8	0x78	RO	I2C_device_ID
0xfc	analog_pwc	8	0x06	RW	[2] vpll_en [1] vpix_en [0] analog pwd enable
0xfd	Scalar mode	8	0x00	RW	[1] column scalar mode [0] scalar mode
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6] cm_reset [5] mipi_reset [4] CISCTL_restart_n [3] NA [2:0] page_select 000:page 0 001:page 1 010:page 2 011: page 3
P0:0x03	Exposure[12:8]	5		RO	[7:5] NA [4:0] exposure[12:8]

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P0:0x04	Exposure[7:0]	8		RO	Exposure[7:0], controlled by AEC if AEC is in function
P0:0x05	buf_CISCTL_capt_hb[11:8]	4	0x00	RW	H Blanking
P0:0x06	buf_CISCTL_capt_hb[7:0]	8	0xaa		
P0:0x07	buf_CISCTL_capt_vb[12:8]	5	0x00	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x08	buf_CISCTL_capt_vb[7:0]	8	0x0c		
P0:0x09	buf_CISCTL_capt_row_start[10:8]	3	0x00	RW	Row Start
P0:0x0a	buf_CISCTL_capt_row_start[7:0]	8	0x00	RW	
P0:0x0b	buf_CISCTL_capt_col_start[10:8]	3	0x00	RW	Col start
P0:0x0c	buf_CISCTL_capt_col_start[7:1]	8	0x04	RW	
P0:0x0d	buf_CISCTL_capt_win_height[10:8]	3	0x04	RW	[7:3] NA [2:0] Window height[10:8]
P0:0x0e	buf_CISCTL_capt_win_height[7:0]	3	0xd0	RW	Window height [7:0]
P0:0x0f	buf_CISCTL_capt_win_width[10:8]	8	0x03	RW	[7:3] NA [2:0] Window width [10:8]
P0:0x10	buf_CISCTL_capt_win_width[7:1]	8	0x28	RW	[7:1]window width[7:1] [0]NA
P0:0x17	Analog mode1	8	0x00	RW	[7:2] reserved [1] updown [0] mirror
P0:0x18	Analog mode2	8	0x0a	RW	[7] NA [6] row skip [5] NA [4:0] reserved
P0:0x20	Analog mode3		0x00		
P0:0x24	Driver mode	8	0x55	RW	[7:6] drv_low_data 00: 8mA

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					01: 12mA 10: 16mA 11: 20mA [5:4] sync_drv 00: 4mA 01: 8mA 10: 12mA 11: 16mA [3:2] drv_high_data 00: 8mA 01: 12mA 10: 16mA 11: 20mA [1:0] pclk_drv 00: 8mA 01: 12mA 10: 16mA 11: 20mA

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_ mode1	8	0x00	RW	[7]clk lane_p2s_sel [6] CTD_lan1 [5] CTD_lane0 [4] CTD_clk [2] phy_lane1_en [1] phy_lane0_en [0] phy_clk_en
P3:0x02	DPHY_analog_ mode2	8	0x00	RW	[7]support odd LWC [6:4] lane0_diff [2:0] clk_diff
P3:0x03	DPHY_analog_ mode3	8	0x00	RW	[7] LP low voltage enable [6] lane1_delay [5] lane0_delay [4] clk_delay [2:0] lane1_diff
P3:0x04	FIFO_prog_full_ level[7:0]	8	0xa0	RW	[7:0] FIFO full level[7:0]
P3:0x05	FIFO_prog_full_ level[11:8]	4	0x00	RW	[3:0] FIFO full level[11:8]
P3:0x06	FIFO_mode	8	0x08	RW	[7] MIPI_CLK_MODULE [6] manual_CSI2_up_mode

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					[5]no flop mode set 1 when [3] is 0 [4] FIFO_rst_mode [3] read gate [2] write gate [1] switchread [0] switch write
P3:0x10	BUF_CSI2_mode	8	0x00	RW	[7] lane_enable [6] NA [5] ULP_mode [4] MIPI_enable [3] bit10_swicth [2] RAW8 [1] line_sync_mode [0] double_lane
P3:0x11	LDI_set	8	0x2b	RW	RAW10
P3:0x12	LWC_set[7:0]	8	0x20	RW	LWC set 640x5/4 RAW10
P3:0x13	LWC_set[15:8]	8	0x03	RW	
P3:0x14	SYNC_set	8	0xb8	RW	[7:0] SYNC set
P3:0x15	DPHY_mode	8	0x00	RW	[7:4] trigger mode [7] DATA gate mode [6] half [5] full [4] prog [3] mipi_write_gate_mode [0] clklane_mode
P3:0x16	LP_set	8	0x09	RW	[7:6] hi-Z [3:2] 1 [1:0] 0
P3:0x17	fifo_gate_mode MIPI_wdiv_set	8	0x00	RW	[7:5] fifo_gate_mode [7] write_and_read_gate_mode [6] write_gate_mode [5] read_gate_mode [3:0] MIPI_wdiv_set default 1/2
P3:0x20	T_init_set	8	0x80	RW	more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	38ns ~95ns LP00
P3:0x23	T_CLK_zero_set	8	0x30	RW	[7:0] T_CLK_PRE_set ,more than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	[7:0] T_CLK_PRE_set ,more than 8UI
P3:0x25	T_CLK_POST_s	8	0x10	RW	[7:0] T_CLK_POST_set, 60ns +52UI

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P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	[7:0] T_CLK_TRAIL_set ,60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	[7:0] T_HS_exit_set ,more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	[7:0] T_wakeup_set ,1ms
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	[7:0] T_HS_PREPARE_set,45+4UI ~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	[7:0] T_HS_Zero_se,140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	[7:0] T_HS_TRAIL_set ,60ns
P3:0x30	MIPI_Test	8	0x00	RW	[1:0] MIPI_Test
P3:0x31	MIPI_Test_data0	8	0x96	RW	MIPI_Test_data0
P3:0x32	MIPI_Test_data1	8	0x3a	RW	MIPI_Test_data1
P3:0x33	MIPI_Test_data2	8	0x87	RW	MIPI_Test_data2
P3:0x34	MIPI_Test_data3	8	0xb5	RW	MIPI_Test_data3
P3:0x3f	FIFO_error log	8		RO	FIFO error log
P3:0x40	output_buf_mode1	8	0x00	RW	[7:4] start_mode [3] NA [2:1] delay_half [0] NA
P3:0x41	output_buf_mode2	8	0x00	RW	[2] clk gating [1] pclk_polarity [0] hsync_polarity
P3:0x42	buf_win_width[7:0]	8	0x40	RW	Buffer window width
P3:0x43	buf_win_width[11:8]	8	0x06	RW	

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x80	Block_enable1	8	0x08	RW	[7] reserved [6] gamma enable [5] CC enable [4] Edge enhancement enable [3] Interpolation enable [2] DN enable [1] DD enable [0] Lens-shading correction enable
P0:0x81	Block_enable2	8	0x28	RW	[7] BLK dither mode

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					[6] low light Y stretch enable [5] skin detection enable [4] reserved [3] new skin mode [2] autogray enable [1] reserved [0] BFF test image mode
P0:0x82	Block enable	8	0x00	RW	[7:3] reserved [2] ABS enable [1] AWB enable [0] NA
P0:0x83	Special effect	8	0x00	RW	[7:4] Effect select 1: 00 gray 2: 7f high 3: dark 4: special red 5: green 6: blue 7: yellow 8: ancients 9: solarize 1 [3] Edge map2 [2] Edge map1 [1] fixed CbCr enable [0] inverse color
P0:0x84	Output format	8	0x02	RW	[7] YUV420 row switch [6] YUV420 col switch [5] YUV420_legacy [4:0] output data mode 5'h00 Cb Y Cr Y 5'h01 Cr Y Cb Y 5'h02 Y Cb Y Cr 5'h03 Y Cr Y Cb 5'h04 LSC bypass, C/Y 5'h05 LSC bypass, Y/C 5'h06 RGB 565 5'h0f bypass 10bits 5'h17 switch odd/even column /row to controls output Bayer pattern 00 RGBG 01 RGGB 10 BGGR

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					11 GBRG 5'h18 DNDD out mode 5'h19 LSC out mode 5'h1b EEINTP out mode
P0:0x85	Frame start	8	0x60	RW	Frame start num
P0:0x86	Sync mode	8	0x0f	RW	Synchronize signal output mode [7] data delay half [6] hsync delay half [5] odd even row switch [4] odd even col switch [3] opclk gated in HB 0: not gated 1: gated [2] opclk polarity 0: invert of isp_2pclk(isp_pclk) 1: same as isp_2pclk(isp_pclk) [1] hsync polarity 0: low valid 1: high valid [0] vsync polarity 0: low valid 1: high valid
P0:0x87	block_enable3_buf	1	0x00	RW	[7:1] NA [0] auto_edge_effect
P0:0x88	module_gating	2	0x03	RW	[7:2] NA [1] ctl_auto_gating [0] out_auto_gating
P0:0x89	bypass_mode	8	0x03	RW	[7] YUV_420_mode [6] single_2_double_mode [5] first_second_switch [4] shake_mode [3] 8 bit bypass [2] 10 bit bypass(for 8 bit data line FPGA) [1:0] bypass which 8bits from 11bit, in is 8 bit bypass mode 11: [10:3]----default 10: [9:2] 01: [8:1] 00: [7:0]
P0:0x8c	debug_mode2	8	0x00	RW	[7:5]reserved [4] skin map [3] test image mode

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					1: UXGA 0: VGA [2] input test image [1] LSC test image [0] test image after EEINTP
P0:0x8d	Debug_mode3	8	0x01	RW	[7:4] test image fix value [3] test image fix value mode [2] reserved [1] INBF enable [0] update gain mode
P0:0x90	Crop enable	8	0x00	RW	[7:1] NA [0] Crop out Window mode
P0:0x91	out_win_y1[10:8]	3	0x00	RW	out_win_y1[10:8]
P0:0x92	out_win_y1 [7:0]	8	0x00	RW	out_win_y1[7:0]
P0:0x93	out_win_x1[10:8]	3	0x00	RW	out_win_x1[10:8]
P0:0x94	out_win_x1[7:0]	8	0x00	RW	out_win_x1[7:0]
P0:0x95	out_win_height[10:8]	3	0x04	RW	Out window height[10:8]
P0:0x96	out_win_height[7:0]	8	0xb0	RW	Out window height[7:0]
P0:0x97	out_win_width[10:8]	3	0x06	RW	Out window width[10:8]
P0:0x98	out_win_width[7:0]	8	0x40	RW	Out window width[7:0]
P0:0x99	subsample	8	0x11	RW	[7:4] subsample row ratio [3:0] subsample col ratio
P0:0x9a	Subsample mode	6	0x06	RW	[7] hide clk in the head of hsync en [6] hide clk mode [5] use or cut row 1: use 0: cut [4] use or cut col 1: use 0: cut [3] smooth Y [2] smooth Chroma [1] neighbor average mode [0] subsample extend opclk
P0:0x9b	Sub_row_N1	8	0x02	RW	[7:4] sub row num1 [3:0] sub row num2
P0:0x9c	Sub_row_N2	8	0x04	RW	[7:4] sub row num3 [3:0] sub row num4

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P0:0x9d	Sub_row_N3	8	0x00	RW	[7:4] sub row num5 [3:0] sub row num6
P0:0x9e	Sub_row_N4	8	0x00	RW	[7:4] sub row num7 [3:0] sub row num8
P0:0x9f	Sub_col_N1	8	0x02	RW	[7:4] sub col num1 [3:0] sub col num2
P0:0xa0	Sub_col_N2	8	0x04	RW	[7:4] sub col num3 [3:0] sub col num4
P0:0xa1	Sub_col_N3	8	0x00	RW	[7:4] sub col num5 [3:0] sub col num6
P0:0xa2	Sub_col_N4	8	0x00	RW	[7:4] sub col num7 [3:0] sub col num8
P0:0xc2	output_buf_enable_buf	1	0x00	RW	[4] output_buf_enable

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x3f	dark_current_stable_th	8	0x00	RW	dark_current_stable_th
P0:0x40	Blk_mode1	8	0x2b	RW	[7:2] Reserved [1] dark_current_en [0] offset_en
P0:0x42	BLK_limit_value	8	0xff	RW	When Dark data big than it, while get this to replace it for protect dark data. low align 11bits
P0:0x43	BLK_fame_cnt_TH	8	0x54	RW	[7:4] BLK start not smooth [3:0] output start frame
P0:0x5c	Exp_rate_darkc	8	0x00	RW	Exp_rate_darkc
P0:0x5e	current_G1_offset_odd_ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G1_odd
P0:0x5f	current_G1_offset_even_ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G1_even
P0:0x60	current_R1_offset_odd_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_R1_odd
P0:0x61	current_R1_offset_even_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_R1_even
P0:0x62	current_B1_offset_odd_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_B1_odd
P0:0x63	current_B1_offset_even_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_B1_even

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P0:0x64	current_G2_offset_odd_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G2_odd
P0:0x65	current_G2_offset_even_ ratio	6	0x18	RW	[7:6] NA [5:0] 1.5bits offset_ratio_G2_even
P0:0x66	Dark_current_G1_ ratio	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_G1
P0:0x67	Dark_current_R_ ratio	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_R1
P0:0x68	Dark_current_B_ ratio	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_B2
P0:0x69	Dark_current_G2_ ratio	6	0x20	RW	[7:6] NA [5:0] 1.5bits dark_current_ratio_G2
P0:0x6a	manual_G1_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6b	manual_G1_even_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6c	manual_R1_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6d	manual_R1_even_offset	6	0x00	RW	[7:6] NA [5:0]S5, aligned to lower 8 of 11 bits data
P0:0x6e	manual_B2_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x6f	manual_B2_even_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x70	manual_G2_odd_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x71	manual_G2_even_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
P0:0x72	BLK_DD_th BLK_various_th	8	0xf2	RW	[7:4] BLK_DD_th [3:0] BLK_various_th

GAIN

Address	Name	Width	Default Value	R/W	Description
P0:0xa3	channel_gain_G1_odd	8	0x80	RW	G1 odd Channel gain, float 1.7
P0:0xa4	channel_gain_G1_even	8	0x80	RW	G1 even Channel gain, float 1.7
P0:0xa5	channel_gain_R1_odd	8	0x80	RW	R1 odd Channel gain, float 1.7

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P0:0xa6	channel_gain_R1_even	8	0x80	RW	R1 even Channel gain, float 1.7
P0:0xa7	channel_gain_B2_odd	8	0x80	RW	B2 odd channel gain, float 1.7
P0:0xa8	channel_gain_B2_even	8	0x80	RW	B2 even channel gain, float 1.7
P0:0xa9	channel_gain_G2_odd	8	0x80	RW	G2 odd channel gain, float 1.7
P0:0xaa	channel_gain_G2_even	8	0x80	RW	G2 even channel gain, float 1.7
P0:0xad	R_ratio	8	0x80	RW	R ratio, float 1.7
P0:0xae	G_ratio	8	0x80	RW	G ratio, float 1.7
P0:0xaf	B_ratio	8	0x80	RW	B ratio, float 1.7
P0:0xb0	Global_gain	8	0x40	RW	Global gain, float 4.4
P0:0xb1	Auto_pregain	8	0x20	RO	Controlled by AEC , can be manually controlled when disable AEC
P0:0xb2	Auto_postgain	8	0x40	RO	Controlled by AEC , can be manually controlled when disable AEC
P0:0xb3	AWB_R_gain	8	0x40	RO	AWB R gain float 4.4
P0:0xb4	AWB_G_gain	8	0x40	RO	AWB G gain float 4.4
P0:0xb5	AWB_B_gain	8	0x40	RO	AWB B gain float 4.4

DNDD

Address	Name	Width	Default Value	R/W	Description
P2:0x84	DD_dark_th	6	0x0a	RW	DD_dark_th,2.5
P2:0x85	ASDE_DN_B_slope	4	0x02	RW	ASDE_DN_B_slope
P2:0x89	ASDE_low_luma_value_DD_th2	8	0x20	RW	ASDE_low_luma_value_DD_th2,4.4
P2:0x8a	ASDE_low_luma_value_DD_th3	8	0x20	RW	ASDE_low_luma_value_DD_th3,4.4
P2:0x8b	ASDE_low_luma_value_DD_th4	8	0x20	RW	ASDE_low_luma_value_DD_th4,4.4

INTPEE

Address	Name	Width	Default	R/W	Description

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			Value		
P2:0x90	EEINTP mode 1	8	0x6c	RW	[7]edge1_mode [6]HP3_mode [5]edge2_mode [4]Reserved [3]LP_intp_en [2]LP_edge_en [1]NA [0] half_scale_mode_en
P2:0x91	EEINTP mode 2	8	0x00	RW	[7]HP_mode1 [6]HP_mode2 [5]only 2 direction only two direction H and V [4]NA [3]only_defect_map [2]map_dir [1:0]reserved
P2:0x92	direction_TH1	8	0x48	RW	[7:6] reserved [5:0] Lower Criteria for direction detection
P2:0x93	Direction_TH2	6	0x03	RW	[7:6] NA [5:0] Upper Criteria for direction detection
P2:0x94	diff_HV_mode	8	0x00	RW	[7:4] Diff HV TI TH1 [3:0] Diff HV TI TH2
P2:0x95	direction_diff_TH_mode	8	0x83	RW	[7:4] Direction diff TH1 [3:0] Direction diff TH2
P2:0x96	edge level	8	0x00	RW	[3:2] edge level
P2:0x97	Edge1 effect Edge2 effect	8	0x48	RW	[7:4] edge1 effect [3:0] edge2 effect
P2:0x98	Edge_pos_ratio Edge_neg_ratio	8	0x88	RW	[7:4] pos edge ratio [3:0] neg edge ratio
P2:0x99	Edge1_max Edge1_min	8	0x81	RW	[7:4] edge1 max [3:0] edge1 min
P2:0x9a	Edge2_max Edge2_min	8	0x81	RW	[7:4] edge2 max [3:0] edge2 min
P2:0x9b	Edge1_th Edge2_th	8	0x22	RW	[7:4] edge1 threshold [3:0] edge2 threshold
P2:0x9c	Edge_pos_max Edge_neg_max	8	0xf8	RW	[7:4] Positive edge max [3:0] Negative edge max
P2:0x9d	Edge_effect_scaler	4	0x04	RW	[3:0] edge1_effect_scaler

AUTO_CC

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Address	Name	Width	Default Value	R/W	Description
P2:0xc0	CC_mode	8	0x00	RW	reserved
P2:0xc1	CC_CT1_11	8	0x40	RW	CC_CT1_11
P2:0xc2	CC_CT1_12	8	0x00	RW	CC_CT1_12
P2:0xc3	CC_CT1_13	8	0x00	RW	CC_CT1_13
P2:0xc4	CC_CT1_21	8	0x00	RW	CC_CT1_21
P2:0xc5	CC_CT1_22	8	0x40	RW	CC_CT1_22
P2:0xc6	CC_CT1_23	8	0x00	RW	CC_CT1_23
P2:0xe6	CC_R_offset	8	0x00	RW	CC_R_offset
P2:0xe7	CC_G_offset	8	0x00	RW	CC_G_offset
P2:0xe8	CC_B_offset	8	0x00	RW	CC_B_offset

RGB GAMMA

Address	Name	Width	Default Value	R/W	Description
P2:0x10	Gamma_out1	8	0x0a	RW	Knee0=2
P2:0x11	Gamma_out2	8	0x12	RW	Knee1=4
P2:0x12	Gamma_out3	8	0x19	RW	Knee2=6
P2:0x13	Gamma_out4	8	0x1f	RW	Knee3=8
P2:0x14	Gamma_out5	8	0x2c	RW	Knee4=12
P2:0x15	Gamma_out6	8	0x38	RW	Knee5=16
P2:0x16	Gamma_out7	8	0x42	RW	Knee6=20
P2:0x17	Gamma_out8	8	0x4e	RW	Knee7=24
P2:0x18	Gamma_out9	8	0x63	RW	Knee8=32
P2:0x19	Gamma_out10	8	0x76	RW	Knee9=40
P2:0x1a	Gamma_out11	8	0x87	RW	Knee10=48
P2:0x1b	Gamma_out12	8	0x96	RW	Knee11=56
P2:0x1c	Gamma_out13	8	0xa2	RW	Knee12=64
P2:0x1d	Gamma_out14	8	0xb8	RW	Knee13 =80
P2:0x1e	Gamma_out15	8	0xca	RW	Knee14 = 96
P2:0x1f	Gamma_out16	8	0xd8	RW	Knee15 = 112
P2:0x20	Gamma_out17	8	0xe0	RW	Knee16 = 128
P2:0x21	Gamma_out18	8	0xe8	RW	Knee17 = 144
P2:0x22	Gamma_out19	8	0xf0	RW	Knee18 =160
P2:0x23	Gamma_out20	8	0xf8	RW	Knee19 = 192
P2:0x24	Gamma_out21	8	0xfd	RW	Knee20 = 224
P2:0x25	Gamma_out22	8	0xff	RW	Knee21 = 256

YCP

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Address	Name	Width	Default Value	R/W	Description
P2:0xd0	Global saturation	8	0x40	RW	[7:0] Global saturation, controlled by auto saturation
P2:0xd1	saturation_Cb	8	0x30	RW	[7:0] Cb saturation 3.5bits, 0x20=1.0
P2:0xd2	saturation_Cr	8	0x30	RW	[7:0] Cr saturation 3.5bits, 0x20=1.0
P2:0xd3	luma_contrast	8	0x40	RW	[7:0] Luma contrast, can be adjusted via contrast center 2.6bits, 0x40=1.0
P2:0xd4	Contrast center	8	0x80	RW	[7:0] Contrast center value
P2:0xd5	Luma_offset	8	0x00	RW	[7:0] Add offset on luma value. S7.
P2:0xd6	skin_Cb_center	8	0xec	RW	[7:0] Cb criteria for skin detection.
P2:0xd7	skin_Cr_center	4	0x12	RW	[7:0] Cr criteria for skin detection.
P2:0xd9	Skin brightness mode	8	0xe3	RW	[7:4] skin brightness th1 [3:0] skin brightness th2
P2:0xda	Fixed_Cb	8	0x00	RW	S7, if fixed CbCr function is enabled, current image Cb value will be replace by this value to achieve special effect
P2:0xdb	Fixed_Cr	8	0x00	RW	S7, if fixed CbCr function is enabled, current image Cr value will be replace by this value to achieve special effect

Measure Window

Address	Name	Width	Default Value	R/W	Description
P0:0xec	C_big_win_x0	8	0x04	RW	Big win use by AWB
P0:0xed	C_big_win_y0	8	0x02	RW	
P0:0xee	C_big_win_x1	8	0x30	RW	
P0:0xef	C_big_win_y1	8	0x48	RW	

AEC

Address	Name	Width	Default Value	R/W	Description
P0:0xb6	AEC_enable	1	0x00	RW	[7:1] NA [0] AEC enable
P1:0x01	AEC_x1	8	0x04	RW	[7:0] AEC_x1, X8 local measure window
P1:0x02	AEC_x2	8	0x60	RW	[7:0] AEC_x2, X8 local measure window
P1:0x03	AEC_y1	8	0x02	RW	[7:0] AEC_y1, X8
P1:0x04	AEC_y2	8	0x48	RW	[7:0] AEC_y2, X8
P1:0x05	AEC_center_x	8	0x20	RW	[7:0] AEC_center_x1, X8

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	1				
P1:0x06	AEC_center_x2	8	0x40	RW	[7:0] AEC_center_x2, X8
P1:0x07	AEC_center_y1	8	0x18	RW	[7:0] AEC_center_y1, X8
P1:0x08	AEC_center_y2	8	0x30	RW	[7:0] AEC_center_y2, X8
P1:0x0a	AEC_mode1	8	0x01	RW	[7] NA [6] measure point [5] adjust_max_gain [4] AEC gain mode [3] NA [2] gain mode [1:0] skip mode
P1:0x0b	AEC_mode2	8	0x21	RW	[7] fix target [6:4] AEC take action every N frame [3:0 Reserved
P1:0x0c	AEC_mode3	8	0x01	RW	[7] reserved [6:4] center weight mode [3:2] skin weight mode [1:0]NA
P1:0x0d	AEC_mode4	8	0x00	RW	
P1:0x0e	AEC_high_range	8	0xf2	RW	AEC_high_range
P1:0x0f	AEC_low_range	8	0x20	RW	AEC_low_range
P1:0x13	AEC_target_Y	8	0x50	RW	expected luminance value
P1:0x14	Y_average	8	0x10	RO	Current frame luminance average
P1:0x15	target_Y_limit_from_histogram	8	0x80	RW	target_Y_limit_from_histogram
P1:0x16	AEC_number_limit_high_range	8	0x35	RW	AEC number limit high range
P1:0x18	AEC mode5	8	0x91	RW	[7:4] AEC slow margin [2:0] AEC slow speed
P1:0x19	AEC mode 6	8	0x95	RW	[7:4] AEC fast margin [2:0] AEC fast speed
P1:0x1a	AEC gain mode	8	0x96	RW	Gain change criteria, float 1.7, default use 1.2x
P1:0x1f	AEC_max_pre_dg_gain	8	0x30	RW	AEC_max_pre_dg_gain

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P1:0x20	AEC_max_post_dg_gain	8	0xc0	RW	AEC_max_post_dg_gain
P1:0x25	AEC_anti_flicker_step[12:8]	8	0x01	RW	[7:5]NA [4:0] AEC anti flicker step[12:8]
P1:0x26	AEC_anti_flicker_step[7:0]	8	0x68	RW	AEC anti flicker step[7:0]
P1:0x27	AEC_exp_level_1[12:8]	8	0x04	RW	[7:5] NA [4:0] AEC exp level1[12:8]
P1:0x28	AEC_exp_level_1[7:0]	8	0x38	RW	AEC exp level1[7:0]
P1:0x29	AEC_exp_level_2[12:8]	8	0x05	RW	[7:5] NA [4:0] AEC exp level2[12:8]
P1:0x2a	AEC_exp_level_2[7:0]	8	0xa0	RW	AEC exp level2[7:0]
P1:0x2b	AEC_exp_level_3[12:8]	8	0x09	RW	[7:5] NA [4:0] AEC exp level3[12:8]
P1:0x2c	AEC_exp_level_3[7:0]	8	0xd8	RW	AEC exp level_3[7:0]
P1:0x2d	AEC_exp_level_4[12:8]	8	0x0e	RW	[7:5] NA [4:0] AEC exp level 4[12:8]
P1:0x2e	AEC_exp_level_4[7:0]	8	0x10	RW	AEC exp level 4 [7:0]
P1:0x2f	AEC_exp_level_5[12:8]	8	0x10	RW	[7:5] NA [4:0] AEC exp level 5[12:8]
P1:0x30	AEC_exp_level_5[7:0]	8	0xe0	RW	AEC exp level 5 [7:0]
P1:0x31	AEC_exp_level_6[12:8]	8	0x1c	RW	[7:5] NA [4:0] AEC exp level 6[12:8]
P1:0x32	AEC_exp_level_6[7:0]	8	0x20	RW	AEC exp level 6[7:0]
P1:0x33	AEC_exp_level_7[12:8]	8	0x1c	RW	[7:5] NA [4:0] AEC exp level7[12:8]
P1:0x34	AEC_exp_level_7[7:0]	8	0x20	RW	AEC exp level 7[7:0]
P1:0x35	AEC_max_dg_gain1	8	0x40	RW	5.3bits, AEC max dg gain1
P1:0x36	AEC_max_dg_gain2	8	0x40	RW	5.3bits, AEC max dg gain2
P1:0x37	AEC_max_dg_gain3	8	0x40	RW	5.3bits, AEC max dg gain3
P!:0x38	AEC_max_dg_gain4	8	0x40	RW	5.3bits, AEC max dg gain4

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P1:0x39	AEC_max_dg_gain5	8	0x40	RW	5.3bits, AEC max dg gain5
P1:0x3a	AEC_max_dg_gain6	8	0x40	RW	5.3bits, AEC max dg gain6
P1:0x3b	AEC_max_dg_gain7	8	0x40	RW	5.3bits, AEC max dg gain7
P1:0x3c	AEC_max_exp_level AEC_exp_min_l[12:8]	8	0x20	RW	[6:5] Max level setting [4:0] exp min[12:8]
P1:0x3d	AEC_exp_min_l[7:0]	8	0x04	RW	AEC_exp_min_l[7:0]

AWB

Address	Name	Width	Default Value	R/W	Description
P1:0x50	AWB mode 1	8	0x00	RW	Reserved
P1:0x51	AWB parameter	8	0x80	RW	AWB parameter
P1:0x52	AWB parameter	8	0x01	RW	AWB parameter
P1:0x53	AWB parameter	8	0x80	RW	AWB parameter
P1:0x54	AWB parameter	8	0x0f	RW	AWB parameter
P1:0x55	AWB parameter	8	0x00	RW	AWB parameter
P1:0x56	AWB parameter	8	0x00	RW	AWB parameter
P1:0x57	AWB parameter	8	0x07	RW	AWB parameter
P1:0x58	AWB parameter	4	0x00	RW	AWB parameter
P1:0x59	AWB_PRE_RGB_low	8	0x01	RW	RGB pixel low THD
P1:0x5a	AWB_PRE_RGB_high	8	0xf0	RW	RGB pixel high THD
P1:0x5b	AWB parameter	8	0x00	RW	AWB parameter
P1:0x75	AWB_every_N	8	0x01	RW	[7:2] NA [1:0] AWB_every_N
P1:0x76	AWB_R_gain_	8	0x70	RW	Channel gain limit for R, G, B.

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	limit				Float 2.6
P1:0x77	AWB_G_gain_limit	8	0x58	RW	
P1:0x78	AWB_B_gain_limit	8	0x78	RW	
P1:0x79	AWB_R_gain_out_h_limit	8	0x50	RW	outdoor R high limit
P1:0x7a	AWB_G_gain_out_h_limit	8	0x58	RW	outdoor G high limit
P1:0x7b	AWB_B_gain_out_h_limit	8	0x46	RW	outdoor B high limit
P1:0x7c	AWB_R_gain_out_l_limit	8	0x40	RW	outdoor R low limit
P1:0x7d	AWB_G_gain_out_l_limit	8	0x40	RW	outdoor G low limit
P1:0x7e	AWB_B_gain_out_l_limit	8	0x40	RW	outdoor B low limit

ABS

Address	Name	Width	Default Value	R/W	Description
P1:0x9a	ABS_range_compesate ABS_skip_frame	8	0xf3	RW	[7:4] add dynamic range [2:0] abs adjust every frame
P1:0x9b	ABS_stop_margin	4	0x02	RW	[7:4] NA [3:0] margin for ABS to stop adjustment
P1:0x9c	Y_S_compesate ABS_manual_K	8	0x00	RW	[7:4] Y S compensate [3:0] manual ABS slope adjustment
P1:0x9d	Y_stretch_limit	8	0x40	RW	[7:0] Y stretch limit

LSC

Address	Name	Width	Default Value	R/W	Description
P1:0xa0	LSC_row_x2 LSC_col_x2 LSC_pixel_array_select	8	0x03	RW	[3] LSC_row_x2 [2] LSC_col_x2 [1:0] LSC pixel array select
P1:0xa1	LSC_row_center	8	0x80	RW	LSC row center
P1:0xa2	LSC_col_cente	8	0x80	RW	LSC col center

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	r				
P1:0xa4	LSC_Q1_red_b1_sign LSC_Q1_green_b1_sign LSC_Q1_blue_b1_sign LSC_Q2_red_b1_sign LSC_Q2_green_b1_sign LSC_Q2_blue_b1_sign	8	0x00	RW	[6] LSC_Q1_red_b1_sign [5] LSC_Q1_green_b1_sign [4] LSC_Q1_blue_b1_sign [2] LSC_Q2_red_b1_sign [1] LSC_Q2_green_b1_sign [0] LSC_Q2_blue_b1_sign
P1:0xa5	LSC_Q3_red_b1_sign LSC_Q3_green_b1_sign LSC_Q3_blue_b1_sign LSC_Q4_red_b1_sign LSC_Q4_green_b1_sign LSC_Q4_blue_b1_sign	8	0x00	RW	[6] LSC_Q3_red_b1_sign [5] LSC_Q3_green_b1_sign [4] LSC_Q3_blue_b1_sign [2] LSC_Q4_red_b1_sign [1] LSC_Q4_green_b1_sign [0] LSC_Q4_blue_b1_sign
P1:0xa6	LSC_right_red_b4_sign LSC_right_green_b4_sign LSC_right_blue_b4_sign LSC_left_red_b4_sign LSC_left_green_b4_sign LSC_left_blue_b4_sign	8	0x00	RW	[6] LSC_right_red_b4_sign [5] LSC_right_green_b4_sign [4] LSC_right_blue_b4_sign [2] LSC_left_red_b4_sign [1] LSC_left_green_b4_sign [0] LSC_left_blue_b4_sign
P1:0xa7	LSC_up_red_b4_sign LSC_up_green_b4_sign LSC_up_blue_	8	0x00	RW	[6] LSC_up_red_b4_sign [5] LSC_up_green_b4_sign [4] LSC_up_blue_b4_sign [2] LSC_down_red_b4_sign [1] LSC_down_green_b4_sign

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	b4_sign LSC_down_red_b4_sign LSC_down_green_b4_sign LSC_down_blue_b4_sign				[0] LSC_down_blue_b4_sign
P1:0xa8	LSC_right_up_red_b22_sign LSC_right_up_green_b22_sign LSC_right_up_blue_b22_sign LSC_right_down_red_b22_sign LSC_right_down_green_b22_sign LSC_right_down_blue_b22_sign	8	0x00	RW	[6] LSC_right_up_red_b22_sign [5] LSC_right_up_green_b22_sign [4] LSC_right_up_blue_b22_sign [2] LSC_right_down_red_b22_sign [1] LSC_right_down_green_b22_sign [0] LSC_right_down_blue_b22_sign
P1:0xa9	LSC_left_up_red_b22_sign LSC_left_up_green_b22_sign LSC_left_up_blue_b22_sign LSC_left_down_red_b22_sign LSC_left_down_green_b22_sign LSC_left_down_blue_b22_sign	8	0x00	RW	[6] LSC_left_up_red_b22_sign [5] LSC_left_up_green_b22_sign [4] LSC_left_up_blue_b22_sign [2] LSC_left_down_red_b22_sign [1] LSC_left_down_green_b22_sign [0] LSC_left_down_blue_b22_sign
P1:0xaa	LSC_Q1_red_b1	8	0x20	RW	LSC Q1 red b1
P1:0xab	LSC_Q1_green_b1	8	0x20	RW	LSCQ1 green b1
P1:0xac	LSC_Q1_blue_b1	8	0x20	RW	LSC Q1 blue b1
P1:0xad	LSC_Q2_red_b	8	0x20	RW	LSC Q2 red b1

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	1				
P1:0xae	LSC_Q2_green_b1	8	0x20	RW	LSC Q2 green b1
P1:0xaf	LSC_Q2_blue_b1	8	0x20	RW	LSC Q2 blue b1
P1:0xb0	LSC_Q3_red_b1	8	0x20	RW	LSC Q3 red b1
P1:0xb1	LSC_Q3_green_b1	8	0x20	RW	LSC Q3 green b1
P1:0xb2	LSC_Q3_blue_b1	8	0x20	RW	LSC Q3 blue b1
P1:0xb3	LSC_Q4_red_b1	8	0x20	RW	LSC Q4 red b1
P1:0xb4	LSC_Q4_green_b1	8	0x20	RW	LSC Q4 green b1
P1:0xb5	LSC_Q4_blue_b1	8	0x20	RW	LSC Q4 blue b1
P1:0xb6	LSC_right_red_b2	8	0x20	RW	LSC right red b2
P1:0xb7	LSC_right_green_b2	8	0x20	RW	LSC right green b2
P1:0xb8	LSC_right_blue_b2	8	0x20	RW	LSC right blue b2
P1:0xb9	LSC_right_red_b4	8	0x20	RW	LSC right red b4
P1:0xba	LSC_right_green_b4	8	0x20	RW	LSC right green b4
P1:0xbb	LSC_right_blue_b4	8	0x20	RW	LSC right blue b4
P1:0xbc	LSC_left_red_b2	8	0x20	RW	LSC left red b2
P1:0xbd	LSC_left_green_b2	8	0x20	RW	LSC left green b2
P1:0xbe	LSC_left_blue_b2	8	0x20	RW	LSC left blue b2
P1:0xbf	LSC_left_red_b4	8	0x20	RW	LSC left red b4
P1:0xc0	LSC_left_green_b4	8	0x20	RW	LSC left green b4
P1:0xc1	LSC_left_blue_b4	8	0x20	RW	LSC left blue b4
P1:0xc2	LSC_up_red_b	8	0x20	RW	LSC up red b2

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	2				
P1:0xc3	LSC_up_green_b2	8	0x20	RW	LSC up green b2
P1:0xc4	LSC_up_blue_b2	8	0x20	RW	LSC up blue b2
P1:0xc5	LSC_up_red_b4	8	0x20	RW	LSC up red b4
P1:0xc6	LSC_up_green_b4	8	0x20	RW	LSC up green b4
P1:0xc7	LSC_up_blue_b4	8	0x20	RW	LSC up blue b4
P1:0xc8	LSC_down_red_b2	8	0x20	RW	LSC down red b2
P1:0xc9	LSC_down_green_b2	8	0x20	RW	LSC down green b2
P1:0xca	LSC_down_blue_b2	8	0x20	RW	LSC down blue b2
P1:0xcb	LSC_down_red_b4	8	0x20	RW	LSC down red b4
P1:0xcc	LSC_down_green_b4	8	0x20	RW	LSC down green b4
P1:0xcd	LSC_down_blue_b4	8	0x20	RW	LSC down blue b4
P1:0xd0	LSC_right_up_red_b22	8	0x20	RW	LSC Q1 red b22
P1:0xd1	LSC_right_up_green_b22	8	0x20	RW	LSC Q1 green b22
P1:0xd2	LSC_right_up_blue_b22	8	0x20	RW	LSC Q1 blue b22
P1:0xd3	LSC_right_down_red_b22	8	0x20	RW	LSC Q4 red b22
P1:0xd4	LSC_right_down_green_b22	8	0x20	RW	LSC Q4 green b22
P1:0xd5	LSC_right_down_blue_b22	8	0x20	RW	LSC Q4 Blue b22
P1:0xd6	LSC_left_up_red_b22	8	0x20	RW	LSC Q2 red b22
P1:0xd7	LSC_left_up_green_b22	8	0x20	RW	LSC Q2 green b22
P1:0xd8	LSC_left_up_blue_b22	8	0x20	RW	LSC Q2 blue b22
P1:0xd9	LSC_left_down	8	0x20	RW	LSC Q3 red b22

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	_red_b22				
P1:0xda	LSC_left_down_green_b22	8	0x20	RW	LSC Q3 green b22
P1:0xdb	LSC_left_down_blue_b22	8	0x20	RW	LSC Q3 blue b22
P1:0xdc	LSC_Y_dark_th	8	0x20	RW	LSC_Y_dark_th
P1:0xdd	LSC_Y_dark_slope	8	0x10	RW	LSC_Y_dark_slope
P1:0xdf	LSC_U_B2G_stand[9:8] LSC_FF_fixed_en LSC_FF_hold_en LSC_dark_dec_mode LSC_dark_pixel_select_mode LSC_K_RB_select_mode LSC_K_RB_interp_mode	8	0x1c	RW	[7:6]LSC_U_B2G_stand[9:8] [5]LSC_FF_fixed_en [4]LSC_FF_hold_en [3]LSC_dark_dec_mode [2]LSC_dark_pixel_select_mode [1]LSC_K_RB_select_mode [0]LSC_K_RB_interp_mode

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